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EV 325214172 US

Lateral DMOS Transistor With A Self-Aligned Drain Region

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FIELD OF THE INVENTION

[0001] The invention relates to LDMOS transistor structures and, in particular, to a method for forming an LDMOS transistor with reduced conduction and switching losses.

DESCRIPTION OF THE RELATED ART

[0002] Figure 1 is a cross-sectional view of a conventional N-type lateral double-diffused MOS (LDMOS) transistor. In general, LDMOS transistor 10 includes a polysilicon gate 12, an N+ source region 14 formed in a P-type body region 16, and an N+ drain region 18. Polysilicon gate 12 is insulated from the semiconductor substrate by a thin gate oxide layer. Drain region 18 can be formed in an N-well 17 or in a more heavily doped N-type region, such as an N-Drift region 15. A P+ diffusion region 13 is usually included for making electrical contact to body region 16.

[0003] In LDMOS transistor 10, source region 14 and body region 16 are self-aligned to the left edge of polysilicon gate 12. That is, during the fabrication process to form LDMOS transistor 10, polysilicon gate 12 is defined and then the source region implantation and the body region implantation are preformed using the polysilicon gate as a mask. As thus implanted, the source region dopants and the body region dopants are aligned to the left edge of polysilicon gate 12. After

subsequent heat treatments to diffuse the dopants and anneal the silicon substrate, N+ source region 14 and body region 16 as shown in Figure 1 are formed.

[0004] However, at the drain side of LDMOS transistor 10, the diffusion regions, such as the drain region, and the drain contact structures, such as the drain contact, are not self-aligned to the right edge of the polysilicon gate. When N-Drift region 15 is included, the N-drift region can be formed self-aligned to the right edge of the polysilicon gate. However, drain region 18 is formed spaced apart from the right edge of polysilicon gate 12 to form a drift region between body region 16 and heavily doped N+ drain region 18. Furthermore, a drain contact 11 for making electrical contact to drain region 18 is formed above the drain diffusion region. The contact opening is also made without self-alignment to the polysilicon gate.

[0005] Because the N+ drain region and the drain contact opening are not self-aligned, drain region 18 has to be spaced sufficiently apart from the right edge of polysilicon gate 12 to meet lithography requirements for misalignment tolerance. Furthermore, the distance between polysilicon gate 12 and drain region 18 is also selected to meet the desired gate to drain breakdown voltage requirements, the longer the distance, the larger the breakdown voltage. Due to the misalignment tolerance and breakdown voltage requirements, a lower limit is placed on the distance B between polysilicon gate 12 and drain region 18 and distance B cannot be readily minimized. As a result, the conventional LDMOS transistor has a higher cell pitch. Higher cell pitch is undesirable because it results in a higher device resistance (R_{DS}) as the distance between the drain and the source

of the transistor is larger. Higher cell pitch is also undesirable because the resultant transistor device consumes more silicon area and thus is more costly to fabricate.

[0006] In some conventional LDMOS transistors, the polysilicon gate is extended so that the drain region can be formed self-aligned to the edge of the polysilicon gate. However, such LDMOS structures are undesirable because the poly to drain breakdown voltage becomes very low because of the thin gate oxide layer that separates the polysilicon gate from the drain diffusion region.

[0007] In the LDMOS transistor of Figure 1, an N-Drift diffusion region 15 is included at the drain side of the device. Typically, the N-Drift region is more heavily doped than N-well 17 and functions to lower the device resistance (R_{DS}) of the LDMOS transistor. However, N-Drift region 15 is included typically at the expense of a lower breakdown voltage between the p-type body region and the N-type drain drift region. Specifically, the breakdown voltage between the body and the drain drift region is determined by the doping of the more heavily doped side. Since N-Drift diffusion region is more heavily doped than N-well, when N- Drift diffusion region is included in the LDMOS transistor, the breakdown voltage between the body and the drift region is lowered. For example, the breakdown voltage between the body region and the N-well can be on the order of 80 volts above while the breakdown voltage between the body region and the N-Drift can be only about 20 volts.

[0008] It is generally desirable to reduce the device resistance R_{DS} and also the cell pitch of an LDMOS transistor. The device resistance R_{DS} includes the resistance of the source metal line connected to the source region, the source contact resistance, the source region resistance, the channel resistance, the drain region resistance, the resistance of the drain metal line connected to the drain region, and the drain contact resistance. To reduce the device resistance of an LDMOS transistor, it is often necessary to reduce the dimensions of the structures in the LDMOS transistor.

[0009] Typically, the resistance of the drain region contributes to about 30-40% of the total device resistance and the channel resistance contributes to about another 30%. Therefore, to reduce the device resistance, it is sometimes desirable to reduce the polysilicon length of the LDMOS transistor. However, there is a limit as to how much the polysilicon gate length can be scaled down due to limitations from photo-lithography technology. This is because in the self-aligned process to form the source region and the body region, the photoresist mask for the source and the body implantation is formed centered or with minimum overlap rule for misalignment on the polysilicon gate. If the length of the polysilicon gate is reduced too much, there may not be enough room for the mask to align properly on the top of polysilicon. Thus, the polysilicon gate has to have a minimum length to meet the lithography requirement for the placement of the mask on the polysilicon gate to allow sufficient room for misalignment.

[0010] It is desirable to provide an LDMOS transistor with reduced device resistance, reduced device pitch, including reduction of the channel length of the LDMOS transistor.

SUMMARY OF THE INVENTION

[0011] According to one embodiment of the present invention, an LDMOS transistor includes a body region, a source region, a conductive gate, an alignment structure and a drain region. The body region is of a first conductivity type and formed in a semiconductor layer of a second conductivity type. The source region is of the second conductivity type and formed in the body region. The conductive gate is insulated from the semiconductor layer by a first dielectric layer and overlies the body region. The source region is formed self-aligned to a first edge of the conductive gate. The alignment structure is formed adjacent a second edge, opposite the first edge, of the conductive gate. The alignment structure has a first edge in proximity to the second edge of the conductive gate. The drain region is of the second conductivity type and formed in the semiconductor layer self-aligned to the second edge, opposite the first edge, of the alignment structure.

[0012] In one embodiment, the conductive gate is formed by a first polysilicon layer and the alignment structure is formed by a second polysilicon layer. In another embodiment, the alignment structure is a silicon nitride layer.

[0013] The incorporation of the alignment structure in the LDMOS transistor of the present invention enables self-aligned drain region and/or drain contact opening to be formed.

[0014] The present invention is better understood upon consideration of the detailed description below and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 is a cross-sectional view of a conventional N-type lateral double-diffused MOS (LDMOS) transistor.

[0016] Figure 2 is a cross-sectional view of an LDMOS transistor according to one embodiment of the present invention.

[0017] Figure 3 is a cross-sectional view of two LDMOS transistors formed in a multi-cell array according to one embodiment of the present invention.

[0018] Figure 4 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

[0019] Figure 5 is a cross-sectional view of two LDMOS transistors formed in a multi-cell array according to an alternate embodiment of the present invention.

[0020] Figure 6 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

[0021] Figure 7 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

[0022] Figure 8 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

[0023] Figure 9 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

[0024] Figure 10 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0025] In accordance with the principles of the present invention, an LDMOS transistor includes an alignment structure to allow both the source region and the drain region to be formed in a self-aligned manner. Furthermore, the drain contact opening can also be formed self-aligned to the alignment structure. The LDMOS transistor thus formed can have a smaller cell pitch and therefore a lower device resistance, without degrading other device characteristics such as breakdown voltages. In one embodiment, the alignment structure is a dielectric layer such as a silicon nitride layer. In another embodiment, the LDMOS transistor is fabricated in a double-poly process and the alignment structure is formed using one of the two polysilicon layers. The LDMOS transistor of the present invention can realize reduced specific resistance (the product of device resistance and area of the transistor) by reducing the drain resistance. Moreover, the alignment structure can be used to

reduce the gate-to-drain overlap capacitance, there by improving the switching speed of operation.

[0026] When a polysilicon layer is used to form the alignment structure of the LDMOS transistor of the present invention, the transistor can be fabricated using conventional or commercially available double-poly CMOS or BiCMOS fabrication processes. The alignment structure can be formed using either the poly1 or poly2 layers that are available in a double-poly process. Furthermore, the alignment structure can be formed using either a high sheet resistance polysilicon layer or a low sheet resistance polysilicon layer, as will be described in more detail below. Therefore, another advantage offered by the LDMOS transistor of the present invention is ease of integration into existing fabrication processes.

[0027] Figure 2 is a cross-sectional view of an LDMOS transistor according to one embodiment of the present invention. Referring to Figure 2, N-type LDMOS transistor 20 is built using a double-poly fabrication process where the second polysilicon layer, also referred to as the poly2 layer, is used to form the alignment structure. In the present embodiment, N-type LDMOS transistor 20 is built on a semiconductor layer including an N-type epitaxial layer 26 formed on a p-type silicon substrate 22. In the following description, the semiconductor structure in and on which the LDMOS transistor of the present invention is formed will be collectively referred to as "the semiconductor layer." In the embodiment shown in Figure 2, the semiconductor layer includes N-type epitaxial layer 26 and p-type substrate 22. A buried layer 24 is formed on substrate 22 for isolation. One of ordinary skill in the art would appreciate that the LDMOS

transistor of the present invention can be built on various types of semiconductor layers, such as being built on a P-type epitaxial layer, or built on an N-type substrate directly without the use of an epitaxial layer. Furthermore, the inclusion of buried layer 24 is optional. The exact structural configuration of the semiconductor layer is not critical to the use and practice of the present invention.

[0028] The semiconductor layer of LDMOS transistor 20 can be formed using conventional processing steps. In the present embodiment, a p-type silicon substrate having a resistivity of 5 to 10 ohm-cm forms substrate 22. Then, an N-type buried layer 24 is formed in p-type substrate 22, such as by masking, ion implantation and subsequent anneal. N-type buried layer 24 is optional and is generally included to improve device isolation and latchup immunity. Following the buried layer formation, an epitaxial process is carried out to form an epitaxial layer 26 on substrate 22 in a conventional manner, such as by standard epitaxial growth techniques. In the present embodiment, epitaxial layer 26 is an N-type epitaxial layer having a resistivity of approximately 3 ohm-cm.

[0029] In the present embodiment, LDMOS transistor 20 is formed in an N-Well 28 using conventional processing steps, such as by masking selective regions of epitaxial layer 26, performing ion implantation using the appropriate dopants, and annealing to drive-in the dopants. N-well region 28 is optional and in other embodiments, LDMOS transistor 20 can be formed directly in N-type epitaxial layer 26. However, the use of N-well 28 in transistor 20 has the advantage of lowering the drain resistance of the LDMOS transistor.

[0030] Subsequent to the formation of N-well 28, a first gate oxide layer 29 is formed, such as by conventional thermal oxidation processes, and a first polysilicon (poly1) layer is deposited, such as by using chemical vapor deposition. The first polysilicon layer is patterned and etched to define a polysilicon gate (poly gate) 30 of LDMOS transistor 20. The poly1 layer is typically heavily doped and thus, is a low sheet resistance layer.

[0031] In a double poly process, a second gate oxide layer 31 is formed on the semiconductor layer and on top of the poly1 layer, such as by thermal oxidation. A second polysilicon (poly2) layer is then deposited, such as by using chemical vapor deposition. The second polysilicon layer is patterned and etched to define a polysilicon alignment structure 32 of LDMOS transistor 20. In the present embodiment, the left edge of alignment structure 32 overlaps the right edge of polysilicon gate 30. Also, the poly2 layer used to form alignment structure 32 is a heavily doped N-type polysilicon layer. In other embodiments, alignment structure 32 can be made from a heavily doped P-type polysilicon layer or a lightly doped, high sheet resistance polysilicon layer.

[0032] Depending on the fabrication process, the thickness of first gate oxide layer 29 and the thickness of second gate oxide layer 31 may be the same or may be different. Furthermore, in a dual gate oxide process or in a poly1-to-poly2 capacitor process, the thickness of the oxide between the poly1 and poly2 layer is inherently thicker than the oxide between the poly2 layer and the semiconductor layer due to higher oxidation rate on heavily doped poly1 layer.

[0033] After the poly1 and poly2 layers are deposited and patterned to form gate 30 and alignment structure 32, the source, body and drain diffusion regions of the LDMOS transistor can now be formed. Specifically, an N+ source region 34 and a P-type body (P-body) region 36 are formed by ion-implantation and subsequent anneal/drive-in. Source region 34 and body region 36 are self-aligned to left edge (the source end) of poly gate 30. That is, poly gate 30 is used as a mask for the ion-implantation steps for forming source region 34 and body region 36. An N+ drain region 38 and an N-type drift region 40 are also formed by ion-implantation and subsequent anneal/drive-in. In the present embodiment, N-type drift region 40 is formed using an N-type base diffusion region (N-Base). However, in other embodiments, N-type drift region 40 can be formed as other N-type diffusion region having the desired dopant concentration. In accordance with the present invention, because LDMOS transistor 20 includes alignment structure 32, drain region 38 and N-Base 40 are formed self-aligned to the right edge (the drain end) of alignment structure 32. That is, alignment structure 32 serves as a mask for the ion-implantation steps for forming drain region 38 and N-Base 40.

[0034] In the present embodiment, LDMOS transistor 20 includes N-Base 40 which is more heavily doped than N-Well 28. N-Base 40 is optional and is included to reduce the drain resistance of the transistor. In other embodiments, N-Base 40 may be omitted and N-Well 28 connects the drain region of LDMOS transistor 20 to the body region. As mentioned above, in yet other embodiments, N-well 28 may be omitted also and the N-type epitaxial layer 26 forms the drift region of LDMOS transistor 20 connecting N+ drain region 38 to P-body region 36.

[0035] The ion implantation steps for forming N+ source region 34 and N+ drain region 38 may use the same ion implantation step or separate ion implantations can be performed for the source and drain regions. After the ion implantation steps for forming the N+ source, the p-body and drain regions, an ion implantation step may be carried out to form a P+ body contact region 42 in P-body 36. After all of the ion implantation steps, an anneal or drive-in process can be performed to diffuse the implanted dopants and anneal the semiconductor layer.

[0036] After formation of N+ source region 34, P-body region 36, N+ drain region 38, N-Base 40 and P+ contact region 42, a dielectric layer 44 is deposited to encapsulate the semiconductor layer and the polysilicon layers. Contact openings 46 and 48 are subsequently formed to provide electrical contact to the diffusion regions. Contact openings 46 and 48 can be formed using conventional processing steps, such as by photomasking and dry etching. In the present embodiment, a butting contact 48 is formed for making connection to both N+ source region 34 and P+ contact region 42. In accordance with the present invention, contact opening 46 for making electrical connection to drain region 38 is formed self-aligned to alignment structure 32. That is, the right edge (drain end) of alignment structure 32 defines the left edge of contact opening 46.

[0037] Furthermore, in the present embodiment, drain contact opening 46 straddles the right edge (drain end) of alignment structure 32. When a metallization layer is subsequently formed, such as by deposition and patterning, the drain metal contact 50 electrically connects the polysilicon alignment structure to the drain diffusion region. Because alignment structure 32 is formed

in the poly2 layer and overlaps the poly gate in the poly 1 layer, a large misalignment in the drain contact opening can be tolerated without resulting in the drain contact shorted to poly gate 30. In effect, the poly2 alignment structure 32 shields the poly gate from the drain contact opening.

[0038] When LDMOS transistor 20 is thus formed, the source region and the body region are self-aligned as well as the drain region and the N-base region. Therefore, the only remaining misalignment in LDMOS transistor 20 is the poly1 to poly2 misalignment. A poly1 to poly2 misalignment may result in N-Base 40 being formed apart from body region 36 without abutting the body region. However, such misalignment does not detrimentally impact the performance of the LDMOS transistor as long as N-Well 28 is present to provide an N-type region connecting drain region 38 to P-body 36. In some embodiments, it may be desirable to have the more heavily doped N-base region 40 formed spaced apart from P-body 36 anyway to minimize impact ionization at the junction of N-base and P-body. In this manner, the breakdown voltage between the P-body region and the drain drift region is increased because N-well 28 is lightly doped as compared to N-Base 40. Thus, any poly1 to poly2 misalignment will not have any appreciable impact to the electrical characteristics of the LDMOS transistor. In the embodiment shown in Figure 2, N-base 40 is formed abutting P-body 36. However, this is illustrative only and in other embodiments, N-base 40 may be formed spaced apart from P-body 36.

[0039] In the present embodiment, alignment structure 32 is a heavily doped, low sheet resistance polysilicon layer and is formed overlapping poly gate 30. Thus, an electric field is

formed between poly gate 30 and alignment structure 32 which may result in undesirable capacitive coupling. However, as discussed above, because the poly1 layer used to form poly gate 30 is a heavily doped layer as well, during the oxidation process to form the second gate oxide layer for the poly2 layer, the poly1 layer will oxidize at a faster rate forming a thick oxide layer on top of the poly gate. The thick oxide layer acts as an effective isolation between structures formed in poly1 and poly2 layers.

[0040] In an alternate embodiment of the present invention, the poly2 layer used to form the alignment structure is a lightly doped polysilicon layer. A fabrication process may include a lightly doped polysilicon layer to provide a high sheet resistance layer for forming polysilicon resistors. When alignment structure 32 is formed using a high sheet resistance layer, the capacitive coupling effect is further minimized as the potential across the oxide layer separating the poly gate and the alignment structure is reduced, thereby improving the reliability of the LDMOS transistor thus formed.

[0041] In yet another alternate embodiment of the present invention, the alignment structure is formed using a dielectric layer, such as a silicon nitride layer. When the alignment structure is formed using a dielectric layer, the capacitive coupling effect between the poly gate and the alignment structure is eliminated. The silicon nitride layer can be a standard layer of the fabrication process or a dedicated layer added to a conventional fabrication process.

[0042] The LDMOS transistor of the present invention offers many advantages over conventional LDMOS transistor structures.

First, by incorporating an alignment structure so that the drain region and drain contact opening can be formed in a self-aligned manner, the cell pitch of the LDMOS transistor can be reduced. The LDMOS transistor of the present invention can be formed in less silicon area and thus can be manufactured with reduced cost and improved yield. Also, the use of self-aligned structures eliminates process variations due to misalignment of layers. The LDMOS transistor can thus be manufactured with improved reliability and minimized variations in device electrical characteristics.

[0043] Second, when a polysilicon alignment structure is used, the limitation of minimum poly gate length due to source/body mask/lithography requirements is eliminated and the channel length of the poly gate can be shortened. In the conventional LDMOS transistor, the channel length of the poly gate is limited to a certain minimum length to provide sufficient room for accommodating the P-body mask. As discussed above, in an LDMOS transistor, the source region implant and the body implant are performed self-aligned to the source end of the poly gate. Therefore, the source/body mask (such as a photoresist layer) straddles the poly gate. The minimum channel length is defined by the minimum overlap of the source/body mask over the poly gate and the minimum poly gate length beyond the minimum overlap to provide for misalignment tolerance. However, in accordance with the present invention, the poly gate and the alignment structure form a contiguous structure on which the source/body mask can be formed. Because the entire length of the poly gate and the alignment structure (polysilicon or dielectric) can be used for the placement of the source/body implant mask, a shorter channel

length for the poly gate can be realized while still providing sufficient area to meet lithography requirements of the source/body implant mask.

[0044] Lastly, a significant advantage of the LDMOS transistor of the present invention is the improvement in electrical characteristics of the transistor. By incorporating alignment structure 32 in LDMOS transistor 20 of the present invention, the drain region and drain contact opening are formed self-aligned and the channel length can be reduced. As a result, the overall cell pitch is reduced which has the effect of reducing the specific resistance of the transistor. The specific resistance of the transistor is the product of the device resistance R_{DS} and the area (A) of the transistor. When the specific resistance of the transistor is reduced, conduction loss of the transistor is minimized.

[0045] According to an alternate embodiment, LDMOS transistor 20 of Figure 2 forms a unit cell structure which can be repeated to form an array of interconnected LDMOS transistors. Figure 3 is a cross-sectional view of two LDMOS transistors formed in a multi-cell array according to one embodiment of the present invention. Referring to Figure 3, LDMOS transistor array 60 includes a first LDMOS transistor 62A and a second LDMOS transistor 62B formed by sharing a common drain region 64. Each of transistors 62A and 62B is formed in the same manner as LDMOS transistor 20. An one or two dimensional array of LDMOS transistors can be formed by using the unit cell structure of LDMOS transistor 20 and by forming common drain regions as shown in Figure 3. Because the cell pitch of each transistor unit cell can be made smaller than conventional LDMOS transistors, an array

of LDMOS transistors of the present invention can also be made smaller.

[0046] Figure 4 is a cross-sectional view of an LDMOS transistor according to an alternate embodiment of the present invention. N-type LDMOS transistor 70 can be formed using the same processing steps as LDMOS transistor 20 of Figure 2 and detail processing steps will not be further described. In the alternate embodiment of Figure 4, LDMOS transistor 70 is formed by using the poly1 layer as the alignment structure 72 and the poly2 layer as the poly gate 74. Thus, as shown in Figure 4, the drain end of poly gate 74 overlaps alignment structure 72. In the present embodiment, alignment structure 72 is left floating.

[0047] The unit cell structure of LDMOS transistor 70 can be used to form a multi-cell array of LDMOS transistors. Figure 5 illustrates a multi-cell array 80 of LDMOS transistors formed by LDMOS transistors 82A and 82B sharing a common drain region 84. The multi-cell array 80 of LDMOS transistors can be formed in stripes as an one dimensional array of transistors or in a cellular cell configurations as a two dimensional array of transistors. The poly1 layer used to form the alignment structure can be a high sheet resistance layer or a low sheet resistance layer. Also, the alignment structure can be formed using a dielectric layer.

[0048] Furthermore, in the embodiment shown in Figure 4, alignment structure 72 is left floating. In an alternate embodiment, the alignment structure is formed shorted to the drain metal contact as shown in Figure 6. Furthermore, in the embodiments shown in Figures 4-6, the N-Base region is formed

abutting the P-body region. This configuration is illustrative only. In other embodiments, the N-Base region can be formed spaced apart from the P-body region as shown in Figure 7. In LDMOS transistor 100 of Figure 7, a higher drain to body breakdown voltage can be realized.

[0049] Returning to Figure 4, in LDMOS transistor 70, alignment structure 72 is left floating, that is, not electrically shorted to the drain region. Leaving alignment structure 72 floating provides several advantages. First, the capacitance between the poly gate and the alignment structure is reduced substantially, resulting in faster gate charging at the poly gate and improved switching speed of the transistor. Second, if the drain contact is allowed to straddle the alignment structure, a limited amount of contact misalignment can be tolerated as large misalignment can result in shorting of the contact opening to poly gate 74. Therefore, when the poly1 layer is used to form the alignment structure, it is sometimes preferred that the alignment structure be left floating and the drain contact be formed spaced apart from but aligned to the alignment structure.

[0050] LDMOS transistor 70 offers other advantages over conventional LDMOS transistor structures. First, by forming the poly gate using the poly 2 layer and overlapping the poly1 alignment structure, the gate-to-drain overlap capacitance is reduced. The gate-to-drain overlap capacitance introduces Miller capacitance which results in large switching loss. By significantly reducing the gate-to-drain overlap capacitance, LDMOS transistor 70 can be operated with reduced switching loss. Second, in LDMOS transistor 70, the channel under poly gate 74

includes a thin oxide portion and a thick oxide portion where the poly gate overlaps the alignment structure. The threshold voltage of LDMOS transistor 70 is not altered appreciably by the inclusion of a thick oxide portion because of the concentration gradient of the P-body region. Specifically, because the P-body region is implanted using poly gate 74 as a mask, the subsequent diffusion of the implanted dopants results in a concentration gradient whereby the P-body doping concentration decreases from the N+ source edge towards the P-body edge. Therefore, the P-body doping concentration is higher at the thin oxide portion of the channel and lower at the thick oxide portion of the channel. In operation, poly gate 74 can invert the channel because the higher doping concentration is under the thin oxide portion and the lower doping concentration is under the thick oxide portion. Of course, in other embodiments, LDMOS transistor 70 can be formed where the thin oxide portion of the channel extends throughout the P-body region.

[0051] Figures 8 and 9 are cross-sectional views of LDMOS transistors according to alternate embodiments of the present invention. In the embodiments shown in Figures 8 and 9, the alignment structures are formed directly on the surface of the semiconductor layer and also serve the functions of doping the semiconductor substrate to form the N-Base regions. This process is akin to the poly emitter process used in forming bipolar transistors where a heavily doped polysilicon layer is used to dope the silicon to form a diffusion region underneath the heavily doped emitter poly layer.

[0052] In LDMOS transistor 110 of Figure 8, alignment structure 112 is formed in the poly1 layer and is formed directly

on the semiconductor layer. Alignment structure 112 is a heavily doped polysilicon layer. By placing alignment structure 112 directly on the surface of the semiconductor layer, the dopants incorporated in the alignment structure can diffuse into the semiconductor layer during subsequently anneal process. In this manner, LDMOS transistor 110 is formed as a fully self-aligned transistor where N+ drain region 116 is self-aligned to the right edge (drain end) of alignment structure 112 and N-Base 114 is formed by doping from alignment structure 112 itself.

[0053] LDMOS transistor 120 of Figure 9 is an alternate embodiment of LDMOS transistor 110 of Figure 8 where the poly2 layer is used to form an alignment structure 122. A portion of alignment structure 122 is formed on the surface of the semiconductor structure which is used to dope the semiconductor layer to from N-Base region 124. The remaining portion of the alignment structure overlaps the poly gate formed in the poly1 layer.

[0054] In the embodiments shown in Figures 8 and 9, the drain metal contacts straddle the alignment structures. In other embodiments, the alignment structures can be left floating without being shorted to the drain metal contacts.

[0055] Figure 10 is a cross-sectional view of an LDMOS transistor according to yet another embodiment of the present invention. In LDMOS transistor 130 of Figure 10, an alignment structure 132 is formed using a heavily doped poly2 layer and is formed on the top surface of the semiconductor layer. Furthermore, alignment structure 132 is extended to serve as a drain contact for LDMOS transistor 130. Specifically, the

portion of the heavily doped polysilicon alignment structure that contacts the top surface of the semiconductor layer is used to dope the semiconductor layer to form N-Base region 134 in N-Well 136. A drain contact opening 138 is formed on polysilicon alignment structure 132 and drain metal contact 140 is formed in contact opening 138 for making electrical connection to N-Base 134 through alignment structure 132. In this embodiment, an N+ drain region in the semiconductor layer is eliminated and alignment structure 132 provides a low resistance connection between the drain metal contact and the N-base region in the semiconductor layer. In another embodiment, alignment structure 132 can be formed using the poly1 layer.

[0056] The above detailed descriptions are provided to illustrate specific embodiments of the present invention and are not intended to be limiting. Numerous modifications and variations within the scope of the present invention are possible. For example, in the above described embodiments, the P-body region is formed self-aligned to the source end of the polysilicon gate. In other embodiments, the p-body region can be formed using a diffusion region that is not self-aligned to the source-end of the polysilicon gate. For instance, the p-body region can be formed using a P-Well diffusion region.

[0057] Additionally, while the above embodiments illustrate N-type LDMOS transistors, one of ordinary skill in the art would appreciate that the incorporation of the alignment structure of the present invention can be readily applied to P-type LDMOS transistors. Furthermore, the alignment structure of the present invention can be incorporated in enhancement mode or depletion

mode LDMOS transistors. The present invention is defined by the appended claims.